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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/756,864	01/10/2001	Yoshinori Tanaka	49657-904	6644

7590                    02/03/2003

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[REDACTED] EXAMINER

DICKEY, THOMAS L

[REDACTED] ART UNIT      [REDACTED] PAPER NUMBER

2826

DATE MAILED: 02/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No. 09/756,864	Applicant(s) TANAKA ET AL.
Examiner Thomas L Dickey	Art Unit 2826

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

1) Responsive to communication(s) filed on 09 December 2002.

2a) This action is FINAL.      2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

4) Claim(s) 12, 13, 15, 16 and 21-25 is/are pending in the application.

4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5) Claim(s) \_\_\_\_\_ is/are allowed.

6) Claim(s) 12, 13, 15 and 21-24 is/are rejected.

7) Claim(s) 16 and 25 is/are objected to.

8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on 10 January 2001 is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) The proposed drawing correction filed on \_\_\_\_\_ is: a) approved b) disapproved by the Examiner.  
 If approved, corrected drawings are required in reply to this Office action.

12) The oath or declaration is objected to by the Examiner.

### Priority under 35 U.S.C. §§ 119 and 120

13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. 09/095,612.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
 \* See the attached detailed Office action for a list of the certified copies not received.

14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).  
 a) The translation of the foreign language provisional application has been received.

15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

### Attachment(s)

1) Notice of References Cited (PTO-892)

2) Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_

4) Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_

5) Notice of Informal Patent Application (PTO-152)

6) Other: \_\_\_\_\_

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## DETAILED ACTION

1. The amendment filed on 12/09/02 has been entered.

### ***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 12 stands rejected under 35 U.S.C. 102(b) as being anticipated by TAKAISHI (5,604,696).

Takaishi discloses a semiconductor device including a memory cell region 'X' and a peripheral circuit region 'Y', comprising: a semiconductor substrate 1 having a major surface, an insulating film 21-8, having an upper surface, being formed on the major surface of the semiconductor substrate 1 to extend from the memory cell region 'X' to the peripheral circuit region 'Y', a capacitor lower electrode assembly (part 22 generally), including first and second lower electrodes 22 being adjacent to each other through a part of the insulating film 21, being formed on the major surface of the semiconductor substrate 1 to extend up to a vertical position substantially identical to that of the upper surface of the insulating film 21 in the memory cell region 'X', first and second openings formed in the insulating film 21, and the first and the second lower electrodes

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22 formed within the first and second openings, respectively, the first and second lower electrodes 22 each of a cylindrical shape having an interior region, wherein respective sidewalls of the first and the second lower electrodes 22 are formed to extend in a longitudinal direction with respect to the major surface of the semiconductor substrate 1, each sidewall having a cross-section in the longitudinal direction that is substantially linear, and a capacitor upper electrode 24 being formed on the capacitor lower electrode assembly through a dielectric film 23 to extend onto the upper surface of the insulating film 21-8, the upper electrode 24 being formed on the interior region of each of the first and second electrodes 22, the capacitor lower electrode assembly including a capacitor lower electrode part 22 upwardly extending in opposition to the capacitor upper electrode 24 and having a top surface and a bottom surface, wherein the insulating film 21-8 includes an upper insulating film 21 and a lower insulating film 8 being different in etching rate from each other. Note figures 4I and 4A of Takaishi. Note that claim 12, as amended, duplicates claim 14, now cancelled. Claim 12 stands rejected for the same reasons claim 14 was rejected in paper #13.

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

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A. Claims 13 and 21-23 stand rejected under 35 U.S.C. 103(a) as being unpatentable over TAKAISHI (5,604,696) in view of WANG et al. (5,856,220).

Takaishi discloses all the limitations of claims 21-23 except that the part of the insulating film between adjacent first and second electrodes have a width smaller than the minimum working size formable by photolithography. Note figures 4I and 4A of Takaishi.

However, Wang et al. discloses a method whereby isotropic etching cuts through the insulating film in a pair of cuts to produce a pair of adjacent lower electrodes. The width of the part of the insulating film this method leaves between the adjacent electrodes is wholly independent of the limits of photolithography, because the etch is isotropic and thus penetrates sideways as well as downwards. Note how much smaller the distance between the electrodes in figure 12 is than the lithographic feature (part 64) that set the initial spacing between electrodes in figure 10. The width may be zero, or any number larger than zero. Note figure 10-12 of Wang et al. Therefore, it would have been obvious to a person having skill in the art to reduce wasted space occupied by part of the insulating film by replacing the two dimensionally patterned, lithographically size restricted cylindrical lower electrodes of Takaishi's device with the free form etched lower electrodes such as taught by Wang et al. in order to increase electrode area to thus provide higher capacitance.

Takaishi discloses all the limitations of claim 13 except that a side surface of the capacitor lower electrode has a curved plane. Note figures 4I and 4A of Takaishi.

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However, Wang et al. discloses a method that produces a lower electrode with hemispherical, curved side planes. Note figure 12 of Wang et al. Therefore, it would have been obvious to a person having skill in the art to replace the cylindrical side planes of Takaishi's lower electrode with the hemispherical, curved side planes such as taught by Wang et al. in order to increase electrode area to thus provide better higher capacitance.

**B.** Claim 24 stands rejected under 35 U.S.C. 103(a) as being unpatentable over TAKAISHI (5,604,696) in view of WANG et al. (5,856,220), as applied to claim 21 above, and further in view of the admitted prior art.

Takaishi and Wang discloses all the limitations of claim 16, including a "hard" oxide peripheral circuit element protection film 25 disclosed by Takaishi, except that the capacitor upper electrode extends towards the peripheral circuit, and to provide an upper interlayer isolation film with a contact hole formed therein on the capacitor upper electrode. Note figures 4I and 4A of Takaishi, and figure 12 of Wang et al.

However, the admitted prior art discloses a stack type DRAM capacitor with the upper capacitor electrode 1151 extended towards the peripheral circuit, and which provides an upper interlayer isolation film 1205 disposed over the upper capacitor electrode 1151, with a contact hole 1135 formed therein on the capacitor upper electrode 1151. Note figure 117 of the admitted prior art. Therefore, it would have been obvious to a person having skill in the art to extend the upper electrode of Takaishi and Wang et al.'s DRAM capacitor towards the peripheral circuit, and to provide an upper interlayer isola-

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tion film with a contact hole formed therein on the capacitor upper electrode, along with a peripheral circuit element protection film formed under the insulating film such as taught by the admitted prior art in order to allow electrical access to the upper capacitor electrode in the peripheral region and allow the contact hole to be made by a non-critical etch step to thus provide more efficient manufacture.

C. Claim 15 stands rejected under 35 U.S.C. 103(a) as being unpatentable over TAKAISHI (5,604,696) in view of GONZALEZ et al. (5,168,073).

Takaishi discloses a semiconductor device with all the limitations of claim 15 except the dielectric film being formed between a side surface of the capacitor lower electrode part and the insulating film. Note figures 4I and 4A of Takaishi. However, Gonzalez et al. '073 discloses a dielectric film 115 is formed between the entire side surface of the capacitor lower electrode 90 and the insulating film 75. For this reason it is formed "at least" either a side surface or only a part of the bottom surface of the capacitor lower electrode 90 and the insulating film 75. Note figure 10 of Gonzalez et al. Therefore, it would have been obvious to a person having skill in the art to replace the dielectric film of Takaishi's semiconductor device with the dielectric film being formed between a side surface of the capacitor lower electrode part and the insulating film such as taught by Gonzalez et al. in order to thoroughly insulate the bottom electrode from the top electrode at the corners at the tops of the first and second openings formed in the insulating film to thus provide prevent shorts and misread and/or lost data.

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### ***Response to Arguments***

4. Applicant's arguments filed 12/09/02 have been fully considered but they are not persuasive.

It is argued, at page 3 of the remarks, that "As shown in Figure 42 ... openings ... are formed in both the upper and lower insulating films." However, in response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., an opening in the upper film and another opening in the lower film) are not recited in the rejected claim(s). Claim 12 simply requires "openings formed in the insulating film." Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993)..

It is argued, at page 4 of the remarks, that "Takaishi's device does not provide a number of benefits realized by the present invention." However, since Takaishi's device identically discloses the present invention as claimed, discussion of secondary factors is moot.

It is argued, at page 6 of the remarks, that "It is clear that Wang's device is limited to an insulating film that is wider than the limits of photolithography." However, it is not Wang's device but Wang's method (isotropic etching, where the etch removes insulating material out from under the photolithographic feature) that is cited as rendering claims 21-23 obvious.

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It is argued, at page 8 of the remarks, that "the capacitor of Takaishi, by design, already has the lower and upper electrodes thoroughly insulated." However, this is merely because the capacitor of Takaishi only has upper electrodes in the interior of the lower electrodes. Were upper electrodes, in addition, to adjoin the exterior of the lower electrodes, as they do in Gonzales '073, one of ordinary skill would clearly have been motivated to add the dielectric film being formed between a side surface of the capacitor lower electrode part and the insulating film which is disclosed in Gonzales '073, thoroughly insulate the bottom electrode from the top electrode to thus provide prevent shorts and misread and/or lost data.

It is argued, at page 8 of the remarks, that "In particular to claim 24, generalizations such as 'to provide more efficient manufacture' have routinely been found inadequate for providing the specific motivation required by 35 USC 103." However, the cases tell us that adequate motivation is found on a case-by-case basis. In the case of claim 24, a simple change to an already complexly claimed device should require only minimal motivation, because the change is simple, especially compared to the combination of parts of the device disclosed by the primary reference which meet claim 24 without changes. Furthermore, the reference that discloses the missing limitation describes a device that is very close in structure and function to the device disclosed by the primary reference.

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***Allowable Subject Matter***

5. Claims 16 and 25 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Conclusion***

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

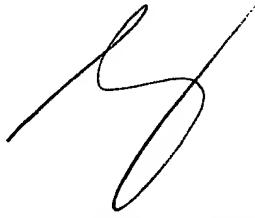
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 703-308-0980. The examiner can normally be reached on Monday through Thursday 8 AM to 6 PM.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 306-3431.

tld  
01/2003



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